Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-2 (cancelled)

Claim 3 (currently amended): A method of forming a microelectronic structure on a semiconductor material having a silicon surface layer on a substrate, comprising the steps of:

a. implanting first dopant ions onto the surface layer;
b. subjecting the semiconductor material to a first annealing process; and
c. subjecting the semiconductor material to a second annealing process, [The method of claim 1] wherein the step of implanting first dopant ions comprises at least one high energy implantation step greater than 200keV, and at least one low energy implantation step less than 5keV.

Claim 4 (original): The method of claim 3, wherein the high-energy ion implantation step is carried out:

a. at an energy level of about 200 keV to about 2000 keV; and
b. with a dosage from $1\times10^{13}/cm^2$ to $1\times10^{17}/cm^2$.

Claims 5-6 (cancelled)

Claim 7 (currently amended): A method of forming a microelectronic structure on a semiconductor material having a silicon surface layer on a substrate, comprising the steps of:

a. implanting first dopant ions onto the surface layer;
b. subjecting the semiconductor material to a first annealing process; and
c. subjecting the semiconductor material to a second annealing process, [The method of claim 1] wherein the second annealing process comprises heating the semiconductor material at a temperature from about 400°C to about 650°C, for a time period from about 1 second to about 10 hours.

Claims 8-14 (cancelled)

Claim 15 (currently amended): A method of forming a microelectronic structure on a semiconductor material by molecular beam epitaxy growth, comprising the steps of

a. exposing, in a vacuum chamber, a single crystal semiconductor body to a flux of one or more atomic or molecular species, with the body maintained at a temperature greater than about 100°C and less than about 800°C;
b. depositing a single crystal epitaxial layer with doped atoms that are electrically active; and
c. subjecting the semiconductor material to a post-growth annealing process, [The method of claim 13] wherein the annealing process comprises heating the semiconductor material with such temperature, amount of time, and heating and cooling rates so that minimal dopant diffusion occurs.